OPAL-RT

OP5000 Signal Conditioning & I/O Products
for RT-LAB Engineering Simulators

# OP5110 Reconfigurable FPGA Platform and I/O Interface

User Manual

OPAL-RT

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# 2 INTRODUCTION

## 2.1 ABOUT THE OP5110 DEVICES

The OP5110-series devices are multifunction digital input/output cards that feature a programmable FPGA chip. Currently, this includes the OP5110-1 and OP5110-2 cards. For most applications, the FPGA chip will have been programmed with dedicated code enabling the features needed for your application. Should these requirements ever change, please contact Opal-RT to see if a programming change could better suit your redefined application.

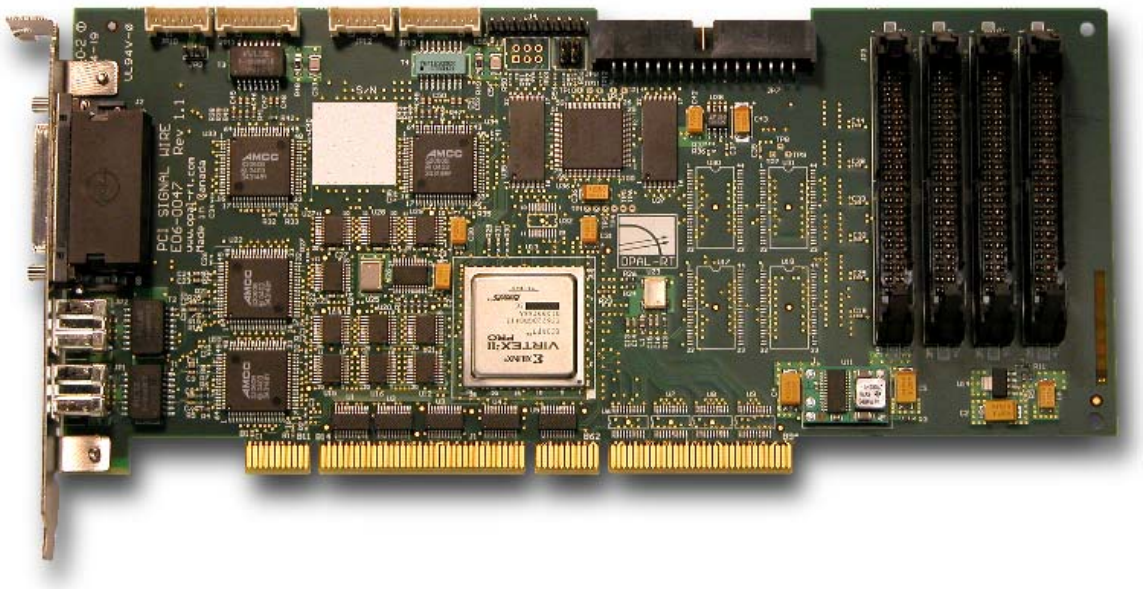


Figure 1: OP5110 Reconfigurable FPGA Platform and I/O Interface

## 2.2 UNPACKING

The OP5110 Reconfigurable FPGA Platform and I/O Interface card is usually not installed in your Engineering Simulator. As the card is usually shipped separately, your OP5110 device should be in an antistatic package to prevent an electrostatic discharge to the device.

An electrostatic discharge can damage several components on the device. To avoid such damage, be sure to follow these important guidelines:

- Ground yourself via a grounding strap or by holding a grounded, metallic object.
- Touch the antistatic package to a metal part of your computer chassis before removing the device from the package.
- Remove the device from the package and inspect the device for loose components or any sign of damage. If the device appears damaged in any way, please notify Opal-RT Technologies. DO NOT install a damaged device in your computer.
- Never touch the exposed pins of connectors.

- When not in use, store your OP5110 device in the antistatic envelope.

### 2.3 Optional Equipment

The OP5100-series cards are designed for use with other OP5000 signal conditioning and interfacing modules. Although stand-alone use is supported, in this manual we assume that the card will be used in an RT-LAB Engineering Simulator.

Typically, this card is used in conjunction with either some OP592x backplane adaptor modules or a SignalWire connection to the OP5912 OPXI Backplane for Type A and B Carriers. For more information on these components, please refer to their respective manuals.

# 3 INSTALLATION AND CONFIGURATION

## 3.1 Hardware Installation

If you need to install the OP5110 card yourself you will need a Phillips #2 screwdriver. After disconnecting all power cables from the computer chassis and opening the case of your system (referred to as the target), you will need to find a free PCI slot. These are usually located at the back or bottom of the PC chassis and feature a slot of multiple connectors in a rectangular connector of about 1cm by 15 cm.

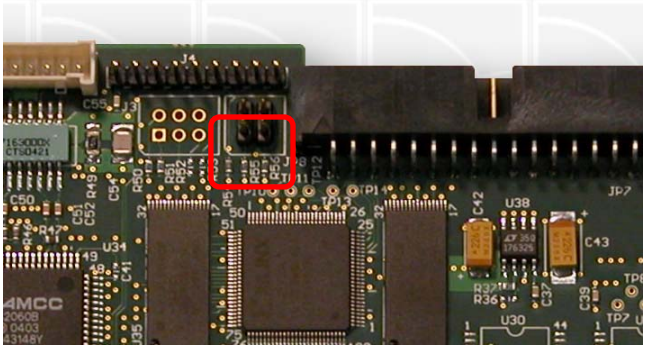
Make sure that there is enough clearance on each side of the OP5110 card once inserted in order for the cable connections to be free of sharp bends and clear of sharp metal parts which could damage the connections.

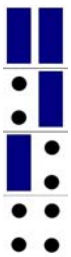
Insert the card by first removing the blank faceplate aligned with the PCI slot on the computer's chassis. Secure the card in its slot by re-using the mounting screw of the faceplate. This should require firm, but not excessive pressure. See appendix E for detailed instructions.

## 3.2 Device Configuration

If your system has multiple OP5110-series cards, each of these must possess a unique board index. Possible board indices range from 12 to 15, with the default board index of 15 being the master card for all other cards in the system most of the time. It is not always the case as the board with index 15 can also be in slave mode. Refer to your system configuration and to your bitstream selection.

The board index is set using the JP8 jumper terminal. By default, the jumpers should be installed on the card so that its board index is set to 15. This is the required setting when there is only one card in the target computer. Other JP8 configurations are used when several cards are installed in the same target and when a master/slave configuration is needed.





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For the clock signal to be propagated from the master card to the other cards, you must connect the clock synchronization cable, as specified in section 5.5.

# 4 DEVICE OVERVIEW

## 4.1 DEVICE DESCRIPTION

The OP5110 card is based around a Xilinx FPGA chip that performs the computational and input/output functionalities. This chip controls 128 digital lines, which can be used, depending on the firmware used, in various configurations.

The card's firmware is a special piece of software that resides onboard and is typically not directly available to the user. This program controls the low-level hardware in order to perform specific task. Each firmware branch supports a different set of input/output configurations. Each configuration is, in turn, a set of base functions using one or more of the FPGA's digital lines.

The next section (4.2) defines the base functionalities, or functional building blocks available. The upcoming *Functionality Matrix* section shows the configurations (combinations of base functionalities) supported by each firmware branch.

## 4.2 FUNCTIONALITY

The functionalities described below are the basic interactions that the card hardware can have with the systems connected to it. In many cases, higher-level applications can be built on top of these low-level functionalities. For each low-level functionality described below, we give a few of the applications that are supported through the RT-LAB software.

### 4.2.1 STATIC DIGITAL INPUT/OUTPUT (SDIO)

The static digital input or output functionality allows you to set or get the state of one of the digital signal lines to one of two discrete values. These values are either a logical "off" level of 0 volts or a logical "on" level of 3.3 volts relative to the card's ground.

These signal lines are named "static" because their state can only be set or read once for every cycle (or computation step) of the simulation. Typical applications of static digital input/output are:

- Switch monitoring/simulation
- Relay driver
- Logical control signals

Note that for the static digital input/outputs, the signals are in groups of 8 lines. A letter ranging from A to P identifies each group. This is the notation used in the RT-LAB blocks that use this functionality.

### 4.2.2 TIME-STAMPED DIGITAL INPUT/OUTPUT (TDIO)

Time-stamped digital inputs and outputs offer the same functionality as the static digital inputs and outputs but, with the added possibility that the signal lines can be toggled or read multiple times and with precise timing during one of the simulation's cycle. This enables you to detect or generate discrete events with precise timing (down to 10ns resolution).

Furthermore, with a higher-level algorithm such as the ones implemented in the RT-LAB and RT-EVENTS block sets, it is possible to use the time-stamped ports for:

- Frequency (square-wave) signal generation/detection
- PWM signal generation/detection
- Quadrature encoder simulation/detection
- Arbitrary digital pulse-train generation and detection

As for the static signals, the time-stamped digital signals are in groups of 8 lines. A letter ranging from A to P identifies each group. This is the notation used in the RT-LAB blocks that use this functionality.

### 4.2.3 PARALLEL INTERFACE TO D/A AND A/D MODULES

In conjunction with an OP5220 Type B I/O Module Carrier (passive), it is possible to use a group of 32 digital signal lines to control and access 16 analog outputs (OP5330 A/D Converter and Signal Conditioning Module) or 16 analog inputs (OP5340 D/A Converter and Signal Conditioning Module).

The access to these analog inputs or outputs is controlled through the corresponding blocks in the RT-LAB block set and allow the following:

- Sensor simulation/reading (temperature, pressure, force, displacement, and much more)
- Actuator control
- Arbitrary waveform playback/detection

### 4.2.4 REFERENCE PULSE GENERATION MODULE (RPG)

The reference pulse generation module allows for the generation of digital events synchronized on a position (angular) reference. The typical use of this module is to generate engine events, such as spark and fuel injection based on an engine's angular position. Note that this is much like the time-stamped digital output functionality, with the generation of events being position-based rather than time-based.

The engine can be simulated in the RPG module. The simulated engine RPM must be given periodically to the RPG core, using its Simulink block. This RPM is used to generate the position pulse train (with 0.1 or 0.01 degrees of precision) and the synchronous events will be generated according to the event specifications given at initialization time.

The RPG module can also be used to generate synchronous events for a real engine. For this, the engine position, CAM and index pulse trains are fed to the RPG module as 0-5 volts signals. Synchronous events will be generated from this external position reference according to the event specifications given at initialization time. The RPG module can perform up sampling of the reference signal, which allows the generation of events within 0.1 or 0.01 degrees of precision with a 1-degree period for the position signal given as input.

### 4.2.5 SIGNALWIRE INTERFACE

SignalWire is a high-speed (625 Mbps) serial data link developed by Opal-RT as a means to link multiple I/O devices together.

When used in conjunction with an OP5130 Type B I/O Module Carrier (active), it is possible to use a group of 32 digital signal lines to control and access 16 analog outputs (OP5330 A/D Converter and Signal Conditioning Module) or 16 analog inputs (OP5340 D/A Converter and Signal Conditioning Module).

Moreover, many application-specific I/O devices are being developed by Opal-RT Technologies which use a SignalWire link to interface with RT-LAB Engineering Simulators.

The access to all these field I/O devices is controlled through the corresponding blocks in the RT-LAB block set and use of the SignalWire serial link is transparent to the user.

## 4.3 FUNCTIONALITY MATRIX

The table that follows shows the various possible configurations for each firmware program available for the OP5110-series cards. Each card shipped is identified with the firmware branch and revision used for its programming. Please use the table to understand the possible combinations of features available to you.

| Device ID | Firmware (S17-0016-PCI prefix) | JP3 (IJKL) | JP4 (MNOP) | JP5 (ABCD) | JP6 (EFGH) | SignalWire |
|---|---|---|---|---|---|---|
| 0x1C | 1C-2 | - | - | ESPG | ESPG | - |
| 0x26 | 0026-27 | 16 D/A | 16 A/D | 16 D/A | 16 A/D | Internal |
| 0x30 | 30-29 | 16 A/D | 16 A/D | 32 TSDIN | 32 TSDOUT | Internal |
| 0x35 | 35-21 | 16 D/A | 16 A/D | 16 TSDIN / 16 TSDOUT | 16 TSDIN / 16 TSDOUT | Internal |
| 0x36 | 36-35 | SPI | - | 16 TSDIN / 16 TSDOUT | - | Internal |
| 0x39 | 39-20 | 16 D/A | 16 D/A | 16 TSDIN 16 TSDOUT | 16 TSDIN / 16 TSDOUT | Internal |

Table 1: Firmware configuration matrix for OP5110-series cards

Note that the last digit of the firmware name is the revision and might be more recent on the card you received. The configurations should nonetheless be identical if the other numbers match those of your card. Note also that the firmware list provided in Table 1 is not exhaustive. Only the most commonly-used and most up-to-date versions are listed.

### 4.3.1 VERIFYING THE FIRMWARE VERSION ON YOUR CARD

The PCI vendor ID for the OP5110 is EDDD. When listing all of the PCI devices in your system, look for this vendor identification to locate the information referring to the OP5110 card. The PCI device ID will refer to the firmware branch (in this case 1A) and the revision displayed will be the revision of the firmware (8 here). All numbers are in hexadecimal representation.

From the QNX command line, using the "`pci -v | less`" will give a listing of all the PCI devices found in you computer system. For Linux, the equivalent command is "`lspci –n –v | less`".

Under QNX (partial listing shown):

```
# pci –v | less

Class             = System Peripherals (Unknown)
Vendor ID         = edddh, Unknown
Device ID         = 1ah, Unknown Unknown
PCI index         = 0h
Revision ID       = 8h
Interrupt line    = 11
```

Under Linux (partial listing shown):

```
# lspci –v –n | less

02:06.0 Class 0880: eddd:001A (rev 08)
        Flags: bus master, medium devsel, latency 0, IRQ 17
        Memory at d0240000 (32-bit, non-prefetchable) [size=256K]
```

# 5 SIGNAL CONNECTIONS

## 5.1 INTERNAL 40-PIN I/O CONNECTORS

| Hardware | | Functionality Mapping | | | |
|---|---|---|---|---|---|
| **Pin#** | **Name** | **Static and Time-Stamped DIO** | **DAC Not Available** | **ADC Not Available** | **RPG (IN / OUT)** |
| 1 | IO0 | A0 | - | - | A0 / Position IN |
| 2 | GND | GND | - | - | GND |
| 3 | IO1 | A1 | - | - | A1 / - |
| 4 | IO2 | A2 | - | - | A2 / Index IN |
| 5 | IO3 | A3 | - | - | A3 / - |
| 6 | IO4 | A4 | - | - | A4 / CAM IN |
| 7 | IO5 | A5 | - | - | A5 / - |
| 8 | IO6 | A6 | - | - | A6 / - |
| 9 | IO7 | A7 | - | - | A7 / - |
| 10 | IO8 | B0 | - | - | B0 / B0 |
| 11 | IO9 | B1 | - | - | B1 / B1 |
| 12 | IO10 | B2 | - | - | B2 / B2 |
| 13 | IO11 | B3 | - | - | B3 / B3 |
| 14 | IO12 | B4 | - | - | B4 / B4 |
| 15 | IO13 | B5 | - | - | B5 / B5 |
| 16 | IO14 | B6 | - | - | B6 / B6 |
| 17 | IO15 | B7 | - | - | B7 / B7 |
| 18 | IO16 | C0 | - | - | C0 / RPG_00 |
| 19 | GND | GND | - | - | GND |
| 20 | - | - | - | - | - |
| 21 | IO17 | C1 | - | - | C1 / RPG_01 |
| 22 | GND | GND | - | - | GND |
| 23 | IO18 | C2 | - | - | C2 / RPG_02 |
| 24 | GND | GND | - | - | GND |
| 25 | IO19 | C3 | - | - | C3 / RPG_03 |
| 26 | GND | GND | - | - | GND |
| 27 | IO20 | C4 | - | - | C4 / RPG_04 |
| 28 | IO21 | C5 | - | - | C5 / RPG_05 |
| 29 | IO22 | C6 | - | - | C6 / RPG_06 |
| 30 | GND | GND | - | - | GND |
| 31 | IO23 | C7 | - | - | C7 / RPG_07 |
| 32 | IO24 | D0 | - | - | D0 / RPG_08 |
| 33 | IO25 | D1 | - | - | D1 / RPG_09 |
| 34 | IO26 | D2 | - | - | D2 / RPG_10 |
| 35 | IO27 | D3 | - | - | D3 / RPG_11 |
| 36 | IO28 | D4 | - | - | D4 / RPG_12 |
| 37 | IO29 | D5 | - | - | D5 / RPG_13 |
| 38 | IO30 | D6 | - | - | D6 / RPG_14 |
| 39 | IO31 | D7 | - | - | D7 / RPG_15 |
| 40 | GND | GND | - | - | GND |

Table 2: Pin Assignment for JP5 Connector

| Hardware | | Functionality Mapping | | | |
|---|---|---|---|---|---|
| **Pin#** | **Name** | **Static and Time-Stamped DIO** | **DAC Not Available** | **ADC Not Available** | **RPG** |
| 1 | IO32 | E0 | - | - | E0 / E0 |
| 2 | GND | GND | - | - | GND |
| 3 | IO33 | E1 | - | - | E1 / E1 |
| 4 | IO34 | E2 | - | - | E2 / E2 |
| 5 | IO35 | E3 | - | - | E3 / E3 |
| 6 | IO36 | E4 | - | - | E4 / E4 |
| 7 | IO37 | E5 | - | - | E5 / E5 |
| 8 | IO38 | E6 | - | - | E6 / E6 |
| 9 | IO39 | E7 | - | - | E7 / E7 |
| 10 | IO40 | F0 | - | - | F0 / C0 |
| 11 | IO41 | F1 | - | - | F1 / C1 |
| 12 | IO42 | F2 | - | - | F2 / C2 |
| 13 | IO43 | F3 | - | - | F3 / C3 |
| 14 | IO44 | F4 | - | - | F4 / C4 |
| 15 | IO45 | F5 | - | - | F5 / C5 |
| 16 | IO46 | F6 | - | - | F6 / C6 |
| 17 | IO47 | F7 | - | - | F7 / C7 |
| 18 | IO48 | G0 | - | - | G0 / D0 |
| 19 | GND | GND | - | - | GND |
| 20 | - | - | - | - | - |
| 21 | IO49 | G1 | - | - | G1 / D1 |
| 22 | GND | GND | - | - | GND |
| 23 | IO50 | G2 | - | - | G2 / D2 |
| 24 | GND | GND | - | - | GND |
| 25 | IO51 | G3 | - | - | G3 / D3 |
| 26 | GND | GND | - | - | GND |
| 27 | IO52 | G4 | - | - | G4 / D4 |
| 28 | IO53 | G5 | - | - | G5 / D5 |
| 29 | IO54 | G6 | - | - | G6 / D6 |
| 30 | GND | GND | - | - | GND |
| 31 | IO55 | G7 | - | - | G7 / D7 |
| 32 | IO56 | H0 | - | - | - / CAM OUT |
| 33 | IO57 | H1 | - | - | - / Index OUT |
| 34 | IO58 | H2 | - | - | - / Position OUT |
| 35 | IO59 | H3 | - | - | - |
| 36 | IO60 | H4 | - | - | - |
| 37 | IO61 | H5 | - | - | - |
| 38 | IO62 | H6 | - | - | - |
| 39 | IO63 | H7 | - | - | - |
| 40 | GND | GND | - | - | GND |

Table 3: Pin Assignment for JP6 Connector

| Hardware | | Functionality Mapping | | | |
|---|---|---|---|---|---|
| **Pin#** | **Name** | **Static and Time-Stamped DIO** | **DAC (A)** | **ADC (A)** | **RPG Not Available** |
| 1 | IO64 | I0 | dac_LDAC0 | adc_CONV0 | - |
| 2 | GND | GND | GND | GND | - |
| 3 | IO65 | I1 | dac_SDI0 | - | - |
| 4 | IO66 | I2 | dac_SDI1 | - | - |
| 5 | IO67 | I3 | SCL | SCL | - |
| 6 | IO68 | I4 | dac_SDI2 | adc_CONV2 | - |
| 7 | IO69 | I5 | dac_LDAC1 | adc_CONV1 | - |
| 8 | IO70 | I6 | SDA | SDA | - |
| 9 | IO71 | I7 | dac_LDAC2 | adc_CONV3 | - |
| 10 | IO72 | J0 | dac_LDAC3 | adc_SDA0 | - |
| 11 | IO73 | J1 | dac_SDI3 | adc_SDB0 | - |
| 12 | IO74 | J2 | adj_SDI1 | adc_SDB1 | - |
| 13 | IO75 | J3 | adj_SDI0 | adc_SDA1 | - |
| 14 | IO76 | J4 | adj_SDI3 | adc_SDA2 | - |
| 15 | IO77 | J5 | adj_SDI2 | adc_SDB2 | - |
| 16 | IO78 | J6 | adj_CLK | adc_SDB3 | - |
| 17 | IO79 | J7 | adj_nCS | adc_SDA3 | - |
| 18 | IO80 | K0 | dac_MSB | adc_A0 | - |
| 19 | GND | GND | GND | GND | - |
| 20 | - | - | - | - | - |
| 21 | IO81 | K1 | dac_nRST | adc_CONV4 | - |
| 22 | GND | GND | GND | GND | - |
| 23 | IO82 | K2 | - | adc_CONV5 | - |
| 24 | GND | GND | GND | GND | - |
| 25 | IO83 | K3 | dac_nCS | adc_nCS | - |
| 26 | GND | GND | GND | GND | - |
| 27 | IO84 | K4 | dac_CLK | adc_CLK | - |
| 28 | IO85 | K5 | - | adc_CONV6 | - |
| 29 | IO86 | K6 | dac_LDAC4 | adc_CONV7 | - |
| 30 | GND | GND | GND | GND | - |
| 31 | IO87 | K7 | dac_SDI4 | - | - |
| 32 | IO88 | L0 | dac_SDI5 | adc_SDA4 | - |
| 33 | IO89 | L1 | - | adc_SDB4 | - |
| 34 | IO90 | L2 | dac_SDI6 | adc_SDB5 | - |
| 35 | IO91 | L3 | dac_LDAC5 | adc_SDA5 | - |
| 36 | IO92 | L4 | - | adc_SDA6 | - |
| 37 | IO93 | L5 | dac_LDAC6 | adc_SDB6 | - |
| 38 | IO94 | L6 | dac_LDAC7 | adc_SDB7 | - |
| 39 | IO95 | L7 | dac_SDI7 | adc_SDA7 | - |
| 40 | GND | GND | GND | GND | - |

Table 4: Pin Assignment for JP3 Connector

| Hardware | | Functionality Mapping | | | |
|---|---|---|---|---|---|
| **Pin#** | **Name** | **Static and Time-Stamped DIO** | **DAC (B)** | **ADC (B)** | **RPG Not Available** |
| 1 | IO96 | M0 | dac_LDAC0 | adc_CONV0 | - |
| 2 | GND | GND | GND | GND | - |
| 3 | IO97 | M1 | dac_SDI0 | - | - |
| 4 | IO98 | M2 | dac_SDI1 | - | - |
| 5 | IO99 | M3 | SCL | SCL | - |
| 6 | IO100 | M4 | dac_SDI2 | adc_CONV2 | - |
| 7 | IO101 | M5 | dac_LDAC1 | adc_CONV1 | - |
| 8 | IO102 | M6 | SDA | SDA | - |
| 9 | IO103 | M7 | dac_LDAC2 | adc_CONV3 | - |
| 10 | IO104 | N0 | dac_LDAC3 | adc_SDA0 | - |
| 11 | IO105 | N1 | dac_SDI3 | adc_SDB0 | - |
| 12 | IO106 | N2 | adj_SDI1 | adc_SDB1 | - |
| 13 | IO107 | N3 | adj_SDI0 | adc_SDA1 | - |
| 14 | IO108 | N4 | adj_SDI3 | adc_SDA2 | - |
| 15 | IO109 | N5 | adj_SDI2 | adc_SDB2 | - |
| 16 | IO110 | N6 | adj_CLK | adc_SDB3 | - |
| 17 | IO111 | N7 | adj_nCS | adc_SDA3 | - |
| 18 | IO112 | O0 | dac_MSB | adc_A0 | - |
| 19 | GND | GND | GND | GND | - |
| 20 | - | - | - | - | - |
| 21 | IO113 | O1 | dac_nRST | adc_CONV4 | - |
| 22 | GND | GND | GND | GND | - |
| 23 | IO114 | O2 | - | adc_CONV5 | - |
| 24 | GND | GND | GND | GND | - |
| 25 | IO115 | O3 | dac_nCS | adc_nCS | - |
| 26 | GND | GND | GND | GND | - |
| 27 | IO116 | O4 | dac_CLK | adc_CLK | - |
| 28 | IO117 | O5 | - | adc_CONV6 | - |
| 29 | IO118 | O6 | dac_LDAC4 | adc_CONV7 | - |
| 30 | GND | GND | GND | GND | - |
| 31 | IO119 | O7 | dac_SDI4 | - | - |
| 32 | IO120 | P0 | dac_SDI5 | adc_SDA4 | - |
| 33 | IO121 | P1 | - | adc_SDB4 | - |
| 34 | IO122 | P2 | dac_SDI6 | adc_SDB5 | - |
| 35 | IO123 | P3 | dac_LDAC5 | adc_SDA5 | - |
| 36 | IO124 | P4 | - | adc_SDA6 | - |
| 37 | IO125 | P5 | dac_LDAC6 | adc_SDB6 | - |
| 38 | IO126 | P6 | dac_LDAC7 | adc_SDB7 | - |
| 39 | IO127 | P7 | dac_SDI7 | adc_SDA7 | - |
| 40 | GND | GND | GND | GND | - |

Table 5: Pin Assignment for JP4 Connector

## 5.2 EXTERNAL 68-PIN I/O CONNECTORS

The JP2 high-density external connector can be used instead of the internal IO connectors JP3-JP6; It gives a more direct access to digital IO lines from the outside of the computer enclosure. This is not supported in all firmware releases. Please contact Opal-RT Technologies support (support@opal-rt.com) for more information.

The "left" and "right" side notations are relative to the connector as viewed from outside the computer case with the top where the securing screw is mounted.

| Left-side 68-pin connector | | |
|---|---|---|
| **Pin #** | **Name** | **Static and Time-Stamped DIO** |
| 1 | GND | GND |
| 2 | GND | GND |
| 3 | GND | GND |
| 4 | GND | GND |
| 5 | GND | GND |
| 6 | GND | GND |
| 7 | GND | GND |
| 8 | GND | GND |
| 9 | GND | GND |
| 10 | GND | GND |
| 11 | GND | GND |
| 12 | GND | GND |
| 13 | GND | GND |
| 14 | GND | GND |
| 15 | GND | GND |
| 16 | GND | GND |
| 17 | GND | GND |
| 18 | GND | GND |
| 19 | GND | GND |
| 20 | GND | GND |
| 21 | GND | GND |
| 22 | GND | GND |
| 23 | GND | GND |
| 24 | GND | GND |
| 25 | GND | GND |
| 26 | GND | GND |
| 27 | +5V | |
| 28 | +5V | |
| 29 | IO68 | I4 |
| 30 | IO70 | I6 |
| 31 | IO72 | J0 |
| 32 | IO74 | J2 |
| 33 | IO76 | J4 |
| 34 | IO78 | J6 |
| 35 | IO40 | F0 |
| 36 | IO41 | F1 |
| 37 | IO42 | F2 |
| 38 | IO43 | F3 |
| 39 | IO44 | F4 |
| 40 | IO45 | F5 |
| 41 | IO46 | F6 |
| 42 | IO47 | F7 |

| Right-side 68-pin connector | | |
|---|---|---|
| **Pin #** | **Name** | **Static and Time-Stamped DIO** |
| 1 | GND | GND |
| 2 | GND | GND |
| 3 | GND | GND |
| 4 | GND | GND |
| 5 | GND | GND |
| 6 | GND | GND |
| 7 | GND | GND |
| 8 | GND | GND |
| 9 | GND | GND |
| 10 | GND | GND |
| 11 | GND | GND |
| 12 | GND | GND |
| 13 | GND | GND |
| 14 | GND | GND |
| 15 | GND | GND |
| 16 | GND | GND |
| 17 | GND | GND |
| 18 | GND | GND |
| 19 | GND | GND |
| 20 | GND | GND |
| 21 | GND | GND |
| 22 | GND | GND |
| 23 | GND | GND |
| 24 | GND | GND |
| 25 | GND | GND |
| 26 | GND | GND |
| 27 | +5V | |
| 28 | +5V | |
| 29 | IO28 | D4 |
| 30 | IO30 | D6 |
| 31 | IO32 | E0 |
| 32 | IO34 | E2 |
| 33 | IO36 | E4 |
| 34 | IO38 | E6 |
| 35 | IO00 | A0 |
| 36 | IO01 | A1 |
| 37 | IO02 | A2 |
| 38 | IO03 | A3 |
| 39 | IO04 | A4 |
| 40 | IO05 | A5 |
| 41 | IO06 | A6 |
| 42 | IO07 | A7 |

| | | | | | | |
|---|---|---|---|---|---|---|
| 43 | IO48 | G0 | | 43 | IO08 | B0 |
| 44 | IO49 | G1 | | 44 | IO09 | B1 |
| 45 | IO50 | G2 | | 45 | IO10 | B2 |
| 46 | IO51 | G3 | | 46 | IO11 | B3 |
| 47 | IO52 | G4 | | 47 | IO12 | B4 |
| 48 | IO53 | G5 | | 48 | IO13 | B5 |
| 49 | IO54 | G6 | | 49 | IO14 | B6 |
| 50 | IO55 | G7 | | 50 | IO15 | B7 |
| 51 | IO56 | H0 | | 51 | IO16 | C0 |
| 52 | IO57 | H1 | | 52 | IO17 | C1 |
| 53 | IO58 | H2 | | 53 | IO18 | C2 |
| 54 | IO59 | H3 | | 54 | IO19 | C3 |
| 55 | IO60 | H4 | | 55 | IO20 | C4 |
| 56 | IO61 | H5 | | 56 | IO21 | C5 |
| 57 | IO62 | H6 | | 57 | IO22 | C6 |
| 58 | IO63 | H7 | | 58 | IO23 | C7 |
| 59 | IO64 | I0 | | 59 | IO24 | D0 |
| 60 | IO65 | I1 | | 60 | IO25 | D1 |
| 61 | IO66 | I2 | | 61 | IO26 | D2 |
| 62 | IO67 | I3 | | 62 | IO27 | D3 |
| 63 | IO69 | I5 | | 63 | IO29 | D5 |
| 64 | IO71 | I7 | | 64 | IO31 | D7 |
| 65 | IO73 | J1 | | 65 | IO33 | E1 |
| 66 | IO75 | J3 | | 66 | IO35 | E3 |
| 67 | IO77 | J5 | | 67 | IO37 | E5 |
| 68 | IO79 | J7 | | 68 | IO39 | E7 |

Table 6: Pin assignment for the JP2 external dual 68-pin connector

## 5.3 INTERNAL SIGNALWIRE CONNECTORS

The internal SignalWire connections are typically used to communicate with an OP5130 FPGA-based Type B I/O Module Carrier. The recommended connection is through shielded twisted-pair cables.

| JP13 SignalWire Connector | |
|---|---|
| **Pin#** | **Name** |
| 1 | GND |
| 2 | RX - |
| 3 | RX + |
| 4 | RX Shield |
| 5 | TX Shield |
| 6 | TX - |
| 7 | TX + |
| 8 | GND |

Table 7: Pin assignment for the JP13 SignalWire connector

## 5.4 EXTERNAL SIGNALWIRE CONNECTORS

The external SignalWire connectors are not currently supported in any of the available firmware branches.

## 5.5 SYNCHRONIZATION CONNECTORS

The synchronization connector JP7 is a 34-pin IDC header connector, which allows the propagation of the clock signal from the master card to the slave cards. In the current generation of cards, only signal RTSI0 is used.

The RTSI0 line is configured as an output for cards in master mode (index 15). Any other board index will put the card in slave mode and RTSI0 becomes an input.

| JP7 Synchronization Connector | |
|---|---|
| **Pin#** | **Name** |
| 19 | GND |
| 20 | RTSI0 |
| 21 | GND |
| 22 | RTSI1 |
| 23 | GND |
| 24 | RTSI2 |
| 25 | GND |
| 26 | RTSI3 |
| 27 | GND |

Table 9: Pin assignment for the JP7 synchronization connector

Alternatively, the JP12 connector can also be used to input or output the synchronization signal. In order to activate the RTSI0 signal on the JP12 connector, the "Auto Detect" pin must be shorted to GND.

| JP12 Synchronization Connector | |
|---|---|
| **Pin#** | **Name** |
| 3 | Auto Detect |
| 4 | RTSI0 |
| 5 | +5V |
| 6 | GND |

Table 10: Pin assignment for the JP12 synchronization connector

# APPENDIX A – SPECIFICATIONS

Digital I/O

Number of channels ..... 128 input/output
Compatibility ..... TTL
Power-on state ..... High impedance
Levels

| Level | Minimum | Maximum |
|---|---|---|
| Input low | 0.0v | 0.8v |
| Input high | 2.0v | 5.5v |
| Output low – 12mA (sink) | 0.0v | 0.4v |
| Output high – 12mA (source) | 2.4v | 3.3v |

For additional signal conditioning and protection, see OP531x specifications.

FPGA

Device ..... Xilinx Virtex II Pro
I/O package ..... 625FF
Available RAM ..... 16 KB (ext. to 2MB)
Clock ..... 62.5, 100MHz
Platform options ..... XC2V1000
Logic slices ..... 5,120
Equivalent logic cells ..... 11,500
Available I/O lines ..... 396

Bus

PCI ..... 32-bit, 33MHz, 1Gbps
64-bit, 66MHz, 4Gbps
Data transfers ..... Interrupt or DMA

I/O connectors

Internal DIO ..... 4 x 40-way header AMP 120613-1
Internal SignalWire ..... 2 x Molex 35362-0810
External DIO ..... 1 x Molex 74337-0011
External SignalWire ..... 2 x Lumberg 2301F90V203

Environmental

Operating temperature ..... 0 - 70°C
Storage temperature ..... -55 - 105°C
Relative humidity ..... 10 - 90%, non-condensing
Maximum altitude ..... 2,000 meters

# APPENDIX B – EXAMPLE WIRING: RT-LAB WANDA

Below is an example of the OP5110 card being used in an RT-LAB Engineering Simulator. In this configuration, it allows for 16 digital inputs, 16 digital outputs, all time-stamped (JP5) as well as 16 DAC (JP3) and 16 ADC (JP4) channels connected in parallel.

The SignalWire port is also used to retrieve another set of 16 DAC channels from another FPGA-based card: the OP5130. The RTSI port allows synchronization between both FPGA cards (OP5110 and OP5130).

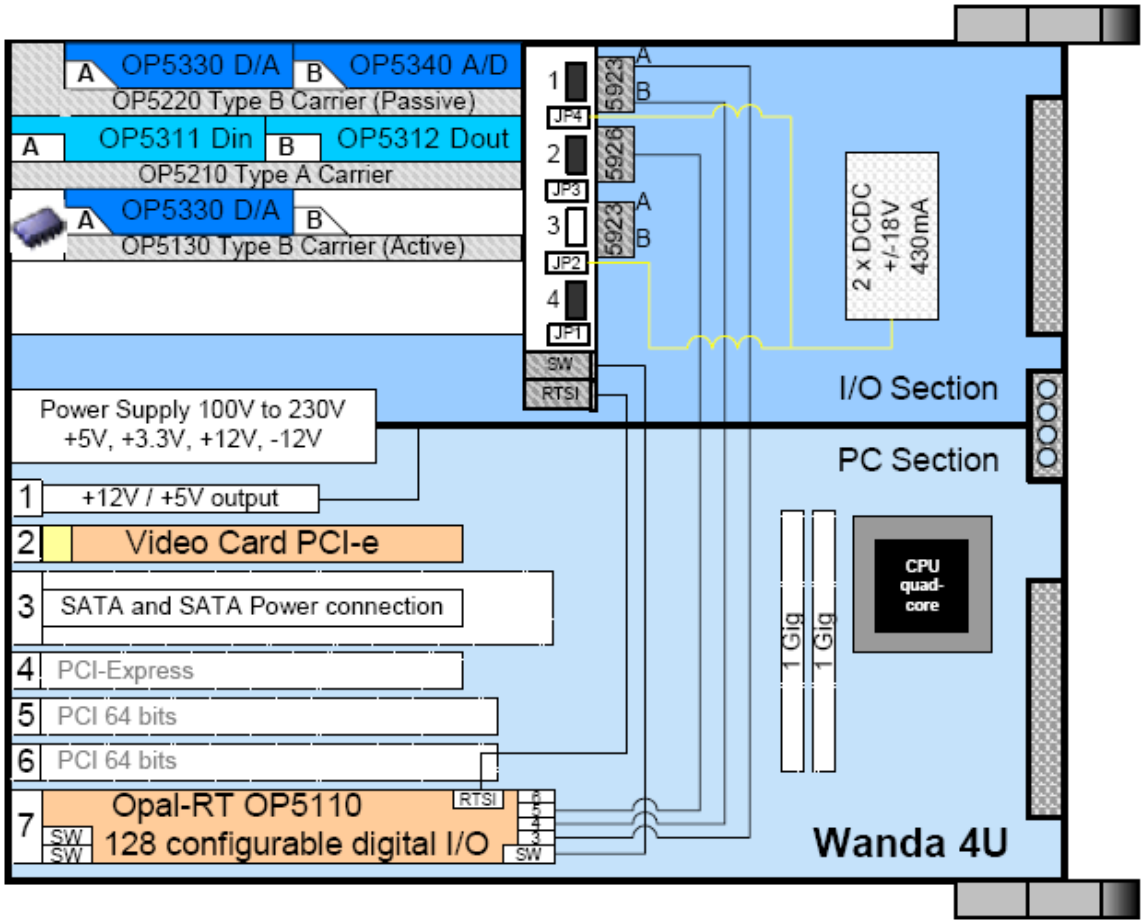



Figure 2: Example wiring of an OP5110 using an RT-LAB Wanda

# APPENDIX C – PORTS IDENTIFICATION

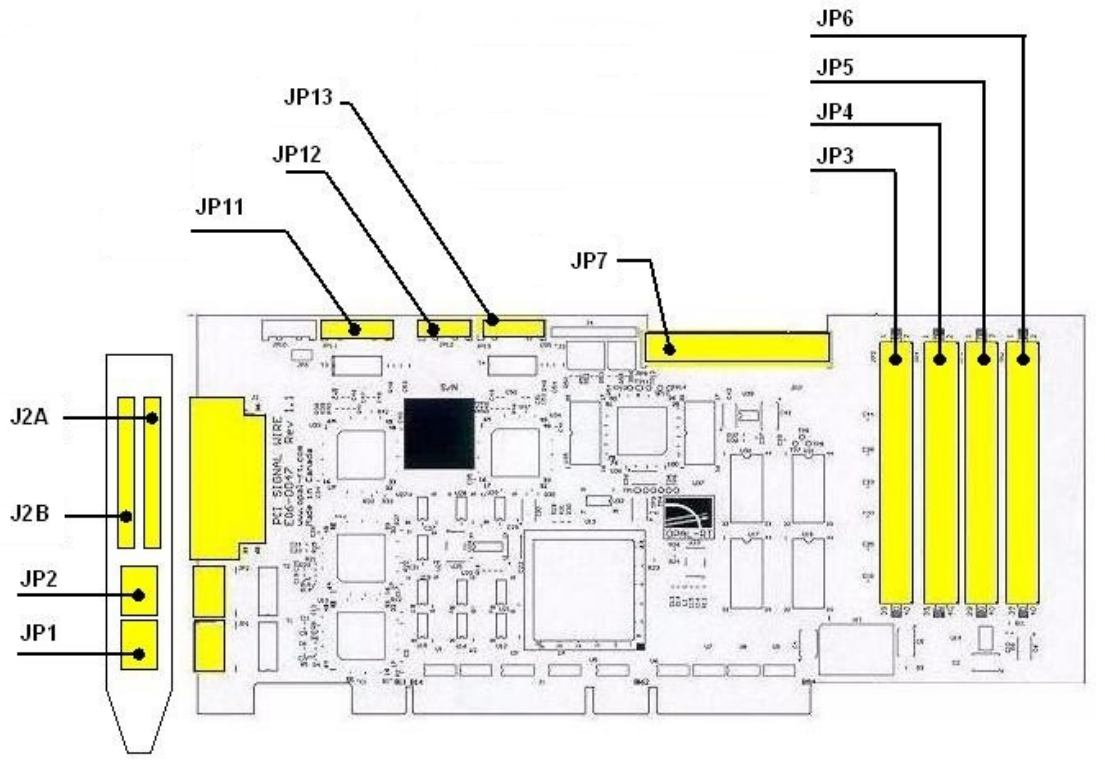



Figure 3: Ports identification of the OP5110.

# APPENDIX D – BLOCK DIAGRAM

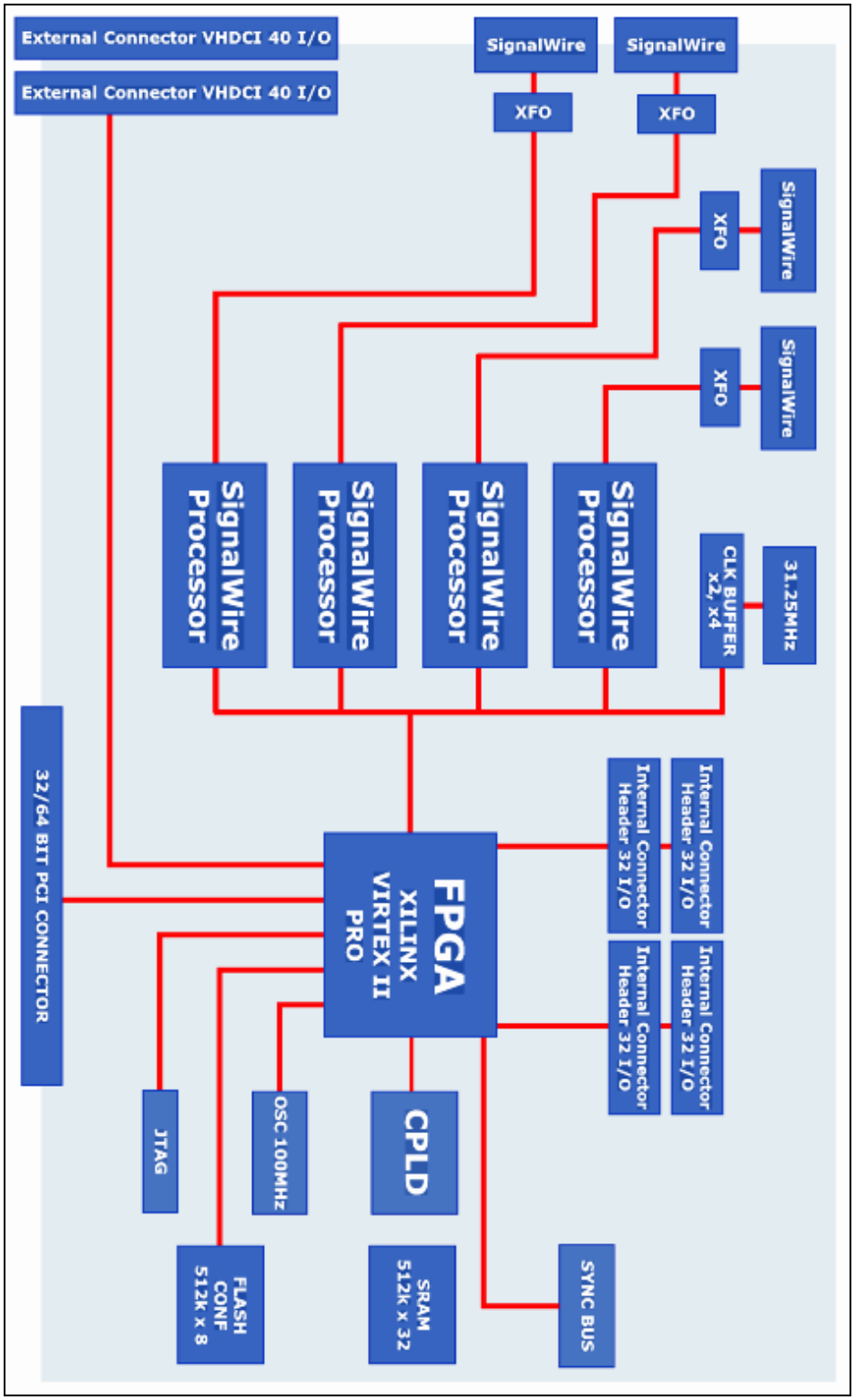



Figure 4: OP5110 Block diagram

# APPENDIX E – OP5110 PCI INSTALLATION GUIDE

## HOW TO INSTALL YOUR FPGA PCI (OP5110 : 126-0158 OR 126-0107)

*Caution: this product is sensitive to static electricity.*

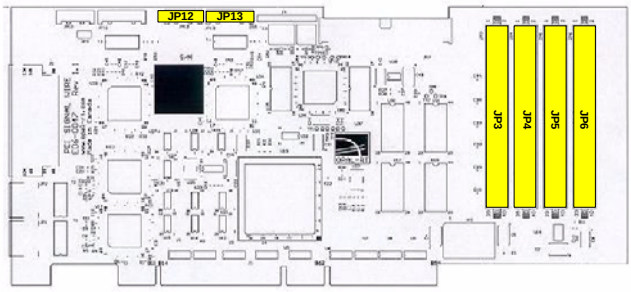
Before you start, be sure the system is not connected to power line.

## Test Drive :

## HIL:

Installation:

- Remove the panel (TestDrive : back panel, HIL : top panel)
- Carrefully insert the PCI card into the empty slot (the one without a bracket) of the target.
- Push the PCI card into the empty slot, so that it is fully seated in the slot.




TestDrive :

- Connect the gray cable to the JP13 connector of the OP5110.
- Secure the bracket, by using the available screw.
- You can now put back the back panel.

HIL :

- If necessary:
  - Connect the flat cable to JP3, JP4, JP5, JP6
  - Installed the signal wire cable to JP13 connectors of the OP5110.
  - Install the Synchronisation cable to JP12 connectors of the OP5110.

  Note: The cable are already inside your system.
- Secure the bracket, by using the available screw.
- You can now put back the top panel.